

REMARKS

Claims 6-20 have been cancelled. Thus, Claims 1-5 are currently pending in the present application, all of which have been amended.

Claims 6-8, 10-14 and 16-20 have been cancelled, and Claims 2-4 have been amended to reflect the correct usage of underlines. Thus, the claim objection is believed to be overcome.

Rejection under 35 U.S.C. § 102

Claims 1-20 were rejected under 35 U.S.C. § 102(a) as being anticipated by *Chow et al.* (PipeRench Implementation of the Instruction Path Coprocessor, IEEE, Dec. 2000). Applicants respectfully traverse such rejection insofar as it might apply to the claims as amended herein.

Amended Claim 1 now recites "means for switching an execution of said legacy code by said CPU to an execution of said plurality of optimized code, in response to an encounter of a switch point." *Chow* does not teach or suggest the claimed switching means. In addition, *Chow* does not teach or suggest the claimed switch point at which execution can be switched from legacy code to optimized code. Because the claimed invention includes novel features that are not taught or suggested by *Chow*, the § 102 rejection is believed to be overcome.

If the Examiner still harbors some doubt as to the novel nature of the claimed invention, Applicants offer to submit an affidavit swearing behind the cited reference.

CONCLUSION

Claims 1-5 are currently pending in the present application. For the reasons stated above, Applicants believe that independent Claim 1 along with its dependent claims are in condition for allowance. The remaining prior art cited by the Examiner but not relied upon has been reviewed and is not believed to show or suggest the claimed invention.

No fee or extension of time is believed to be necessary; however, in the event that any fee or extension of time is required for the prosecution of this application, please charge it against IBM Deposit Account No. **09-0456**.

Respectfully submitted,



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